

# Journal of VLSI Design and Signal Processing

## CONTENTS

| <i>Articles</i>                                                                                                                                                                                                        | <i>Page No.</i> |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|
| 1. <b>Design and Analysis of a New Ultra Low Power Adiabatic VLSI Circuit</b><br><i>Chamak Ganguly, Saeed Hossen Rakib, Farhana Tasnim Aumio, Ariful Islam, S.M. Kifyat Kabir, Raihan Motalib, Satyendra N. Biswas</i> | 1-12            |
| 2. <b>Performance Comparison of Pseudo-p and Complementary OTFT-based Combinational Circuits</b><br><i>T. Marium, S. M. Ishraqul Huq, O. Lowna Baroi, S. Nath Biswas</i>                                               | 13-24           |
| 3. <b>A Novel Channel Routing Using For Minimization of Cross Talk in VLSI</b><br><i>M.L.N. Acharyulu</i>                                                                                                              | 25-38           |
| 4. <b>Development and Realization of a 4x4 Vedic Multiplier Utilizing Cadence Platform</b><br><i>M.V. Tejendra Prasad</i>                                                                                              | 39-51           |
| 5. <b>Implementation of Logarithmic Square Rooter Using Verilog</b><br><i>P. Pavithra</i>                                                                                                                              | 52-59           |



**JOVDSP**