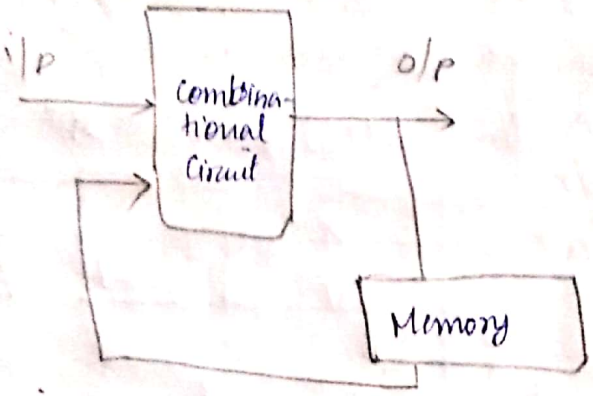
MODULE - II

Combinational circuit

Sequential circuit

present o/p depends on present i/p as well as past output

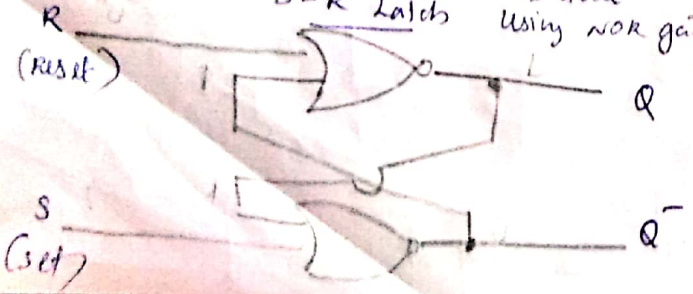
Sequential Circuit



Basic storage element - Latch / Flipflop.
(stores single bit information)

Latch can be implemented using
→ cross coupled - NOR gate / NAND Gate

S-R Latch using NOR gate (Active high)



case 1

S=0, R=1 Q=0 Q̄=1 Reset

S=0, R=0 Q=0, Q̄=1 memory

Set state Q=1, Q̄=0

Reset state Q=0, Q̄=1

NOR

A B	A+B
0 0	1
0 1	0
1 0	0
1 1	0

case 2

S=1, R=0 Q=1 Q̄=0 set

S=0, R=0 Q=1 Q̄=0 memory

Case 3

S=1, R=1, Q=0, Q̄=0.

S=0, R=0, Q=0, Q̄=1. → Indeterminate/invalid

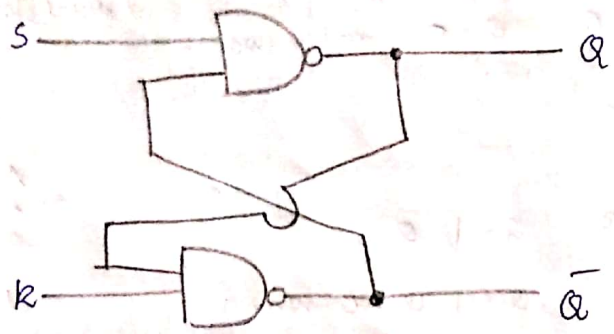
Q=1, Q̄=0.

Truth Table:-

S	R	Q(t+1) (Present o/p)	Q̄(t+1) (Present o/p).	
0	0	Q(t)	Q̄(t)	(Memory)
0	1	0	1	Reset
1	0	1	0	set
1	1	X	X	Indeterminate state.

SR latch using NAND Gate (Active low)

↳ 0 then active



Q(t) — past state

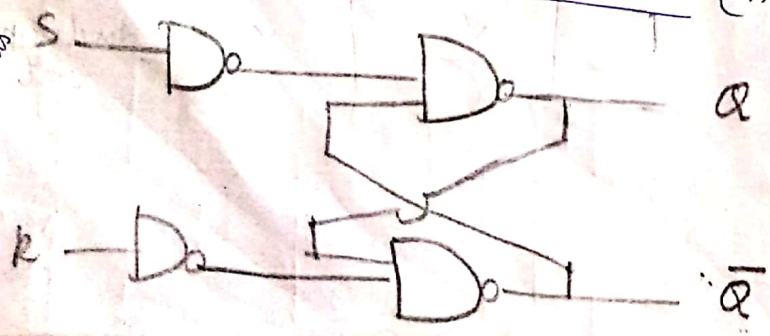
Q(t+1) — present state

S	R	Q(t+1)	$\bar{Q}$(t+1)	
0	0	x	x	Indeterminate
0	1	1	0	set
1	0	0	1	Reset
1	1	Q(t)	$\bar{Q}$(t)	Memory

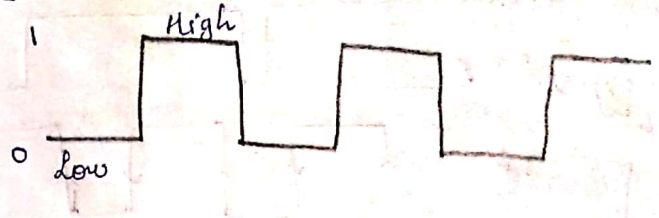
SR latch using NAND Gate (Active high)

↳ 1 then active

Truth table same as



Clock

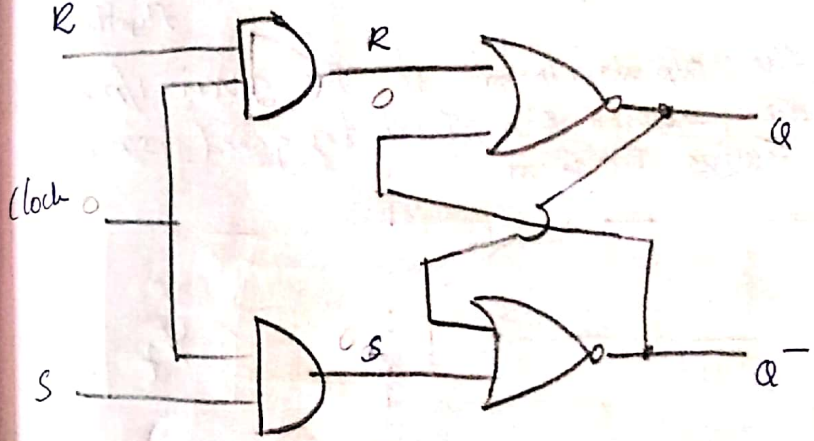


50% duty cycle

If we are using enable line to control — latch

If clock i/p signal — flipflop

S-R flipflop



Latch — Asynchronous

flipflop — Synchronous

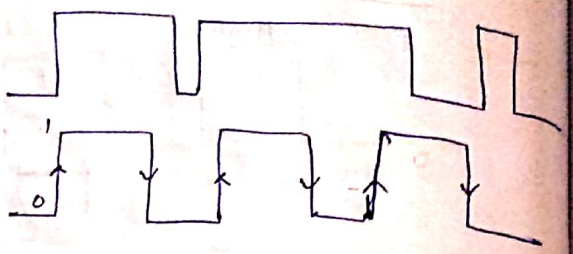
C=0 R&S=0

C=1 R&S value change

Clock	S	R	Q(t+1)
0	x	x	Q(t)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	Indeterminant

Triggering Methods

1. Level Triggered
   Eg:- Latch
2. Edge Triggered
   Eg:- Flipflop

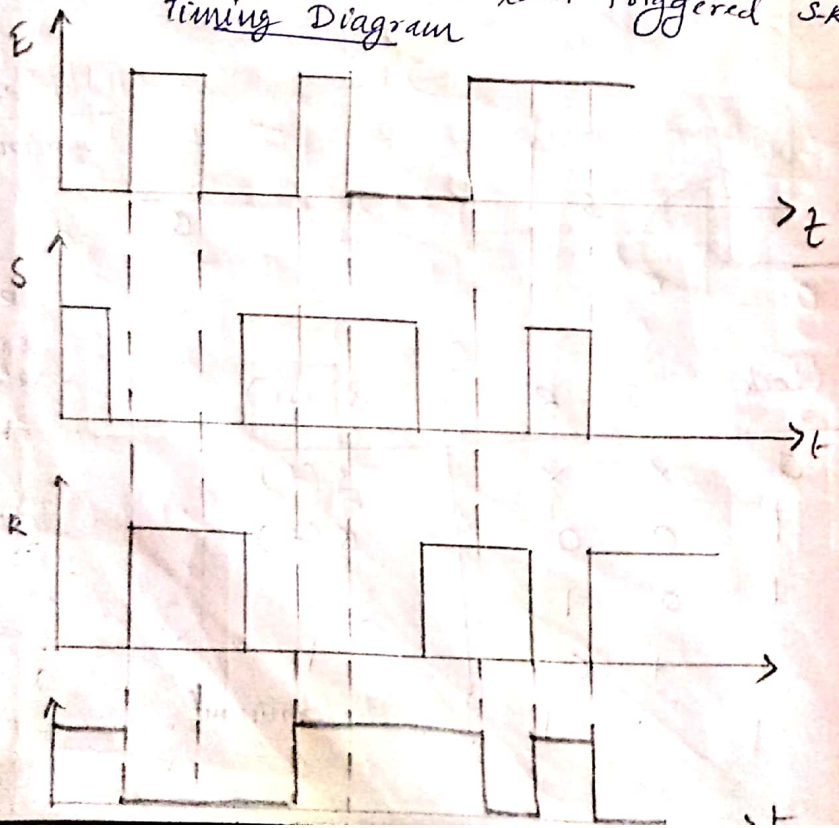


If flipflop is active during +ve edge → +ve edge flipflop

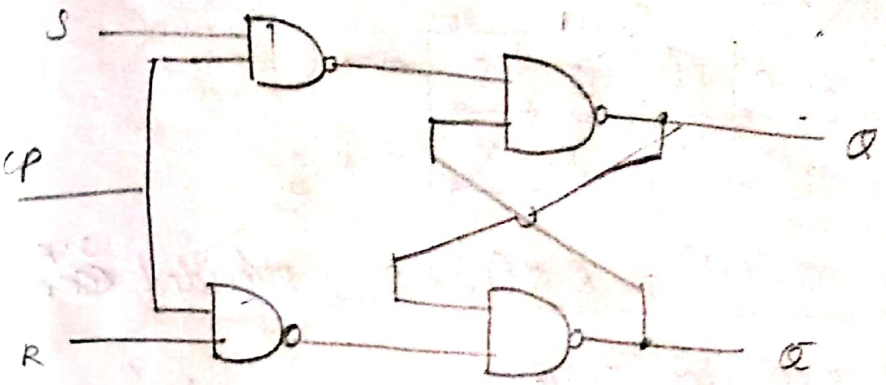
-ve edge → -ve edge flipflop

⇒ Draw the o/p waveform if the given i/p waveforms are applied to a level triggered S-R latch

Timing Diagram



Clocked S-R flipflop / S-R flipflop



Truth Table

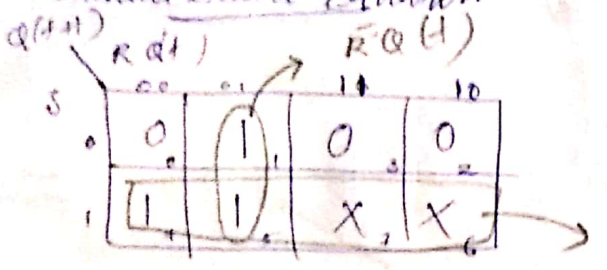
CP	S	R	Q(t+1)	
0	X	X	Q(t)	Memory
1	0	0	Q(t)	
1	0	1	0	
1	1	0	1	
1	1	1	?	Indeterminate state

CP - clock pulse

Characteristic Table

S	R	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Characteristic Equation

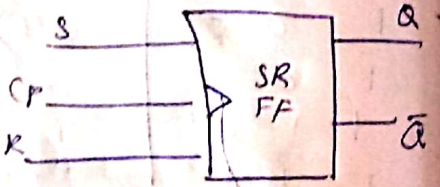


$Q(t+1) = \bar{R}\,Q(t) + S$ provided $S \cdot R = 0$

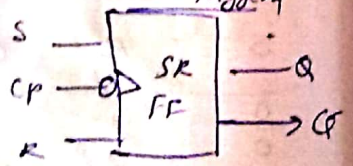
Excitation Table

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

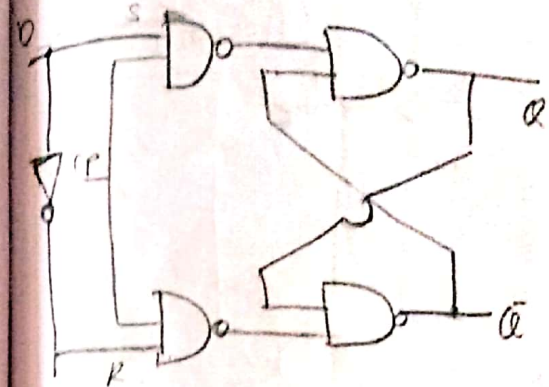
JMP



+ve edge triggered flipflop



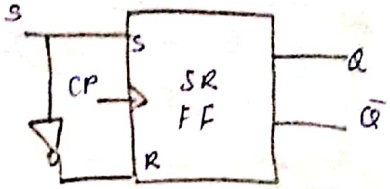
D- flipflop



Excitation Table

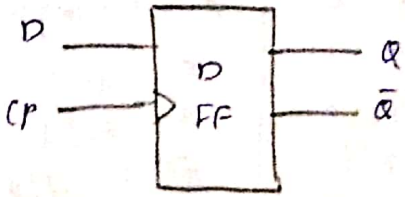
Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Circuit

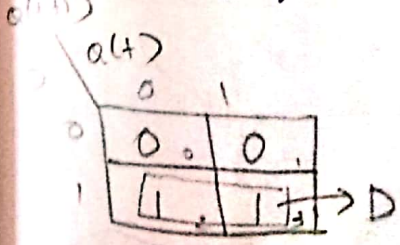


D	Q(t+1)
0	0
1	1

D	Q(t)	Q(t+1)
0	0	0
0	1	0
1	0	1
1	1	1

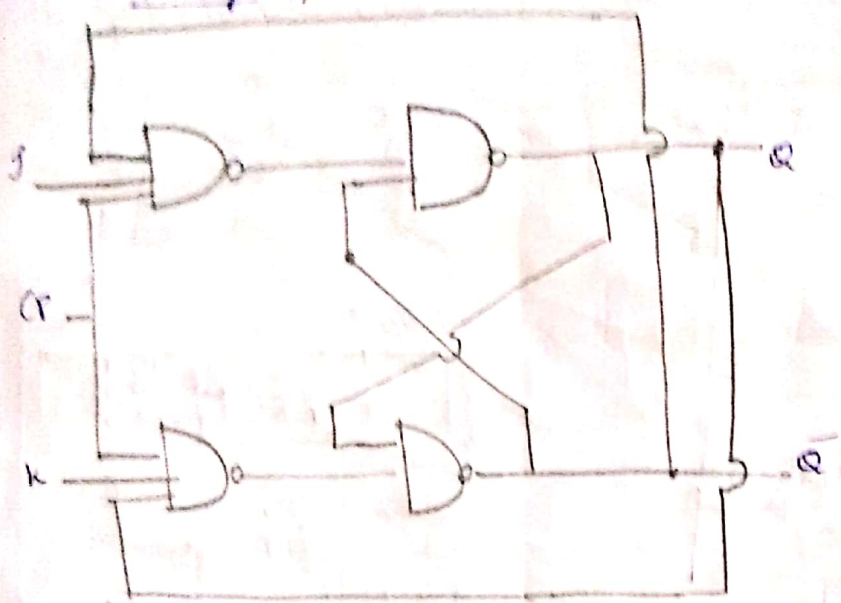


Characteristic equation



$Q(t+1) = D$

JK Flip Flop



Characteristic Table

J	K	Q(t+1)
0	0	Q(t) Memory or hold
0	1	0 - Reset
1	0	1 - Set
1	1	Q̄(t) - Toggle

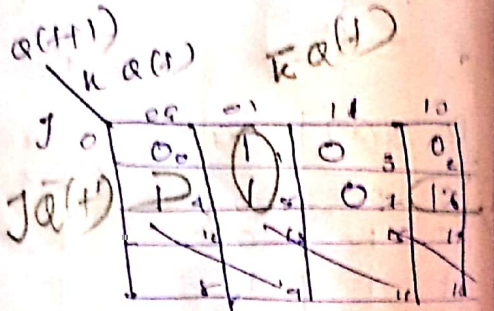
Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Characteristic Table

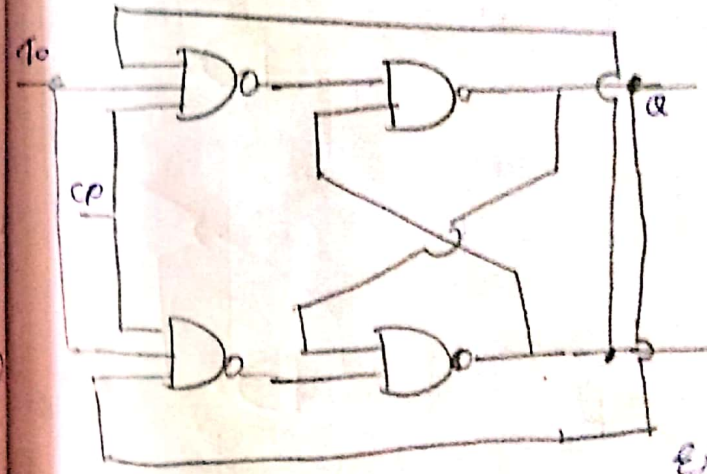
J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic Equation



$$Q(t+1) = J\bar{Q}(t) + \bar{K}Q(t)$$

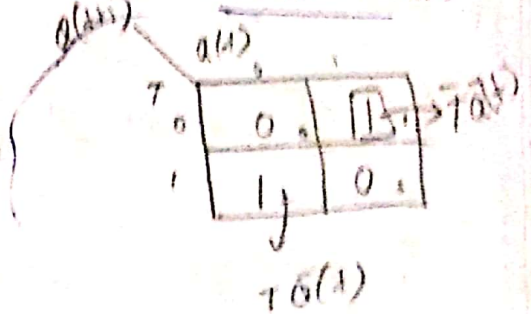
T- Flip Flop



Excitation Table

T	Q(t+1)
0	Q(t)
1	Q̄(t)

Characteristic Equation



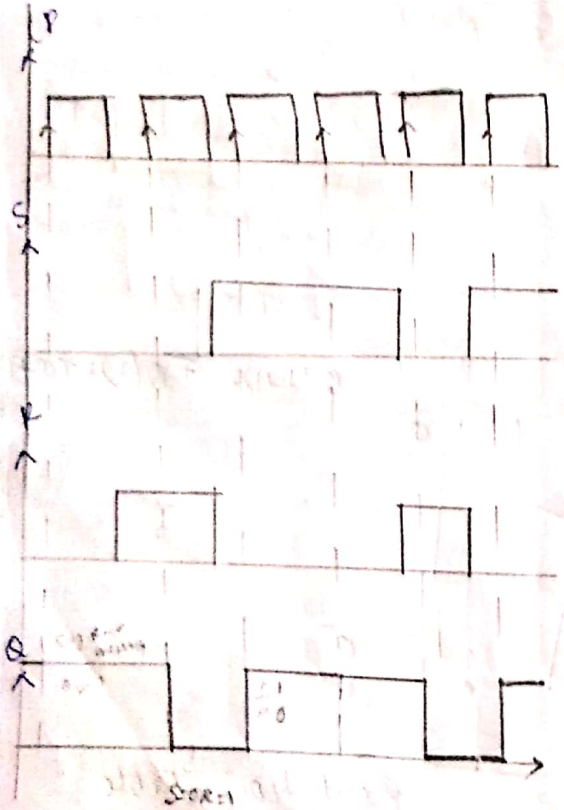
$$Q(t+1) = T\bar{Q}(t) + \bar{T}Q(t)$$

T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

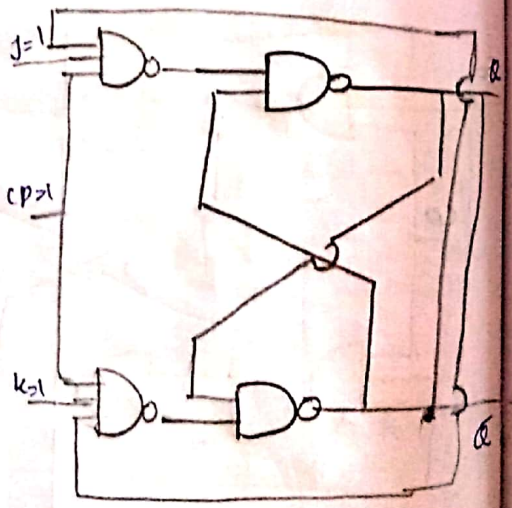
The wave forms shown in the figure are applied to the +ve edge triggered S-R flipflop. Sketch the o/p waveform.



Race Around condition or Racing in JK flipflop

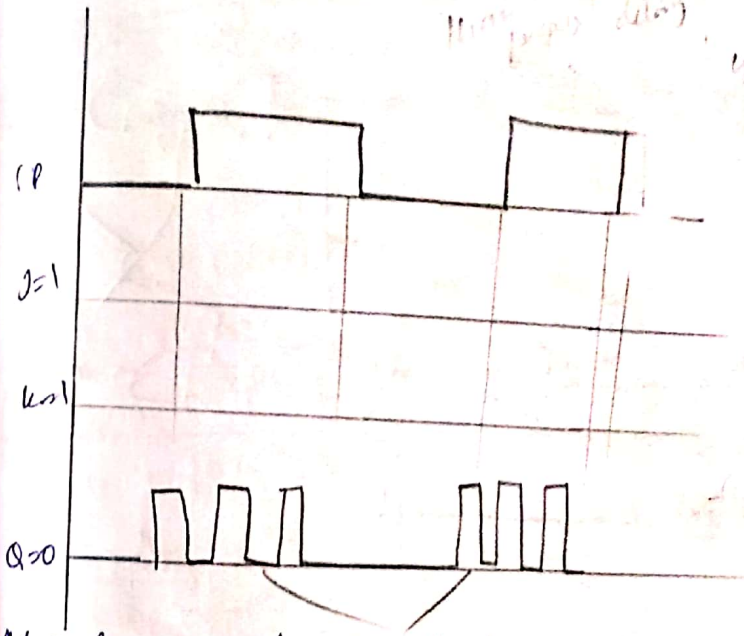
J=1, K=1, CP=1

⇒ Race condition - Repeated and continuous complimentation of o/p is called racing. This because of the feedback in JK flipflop



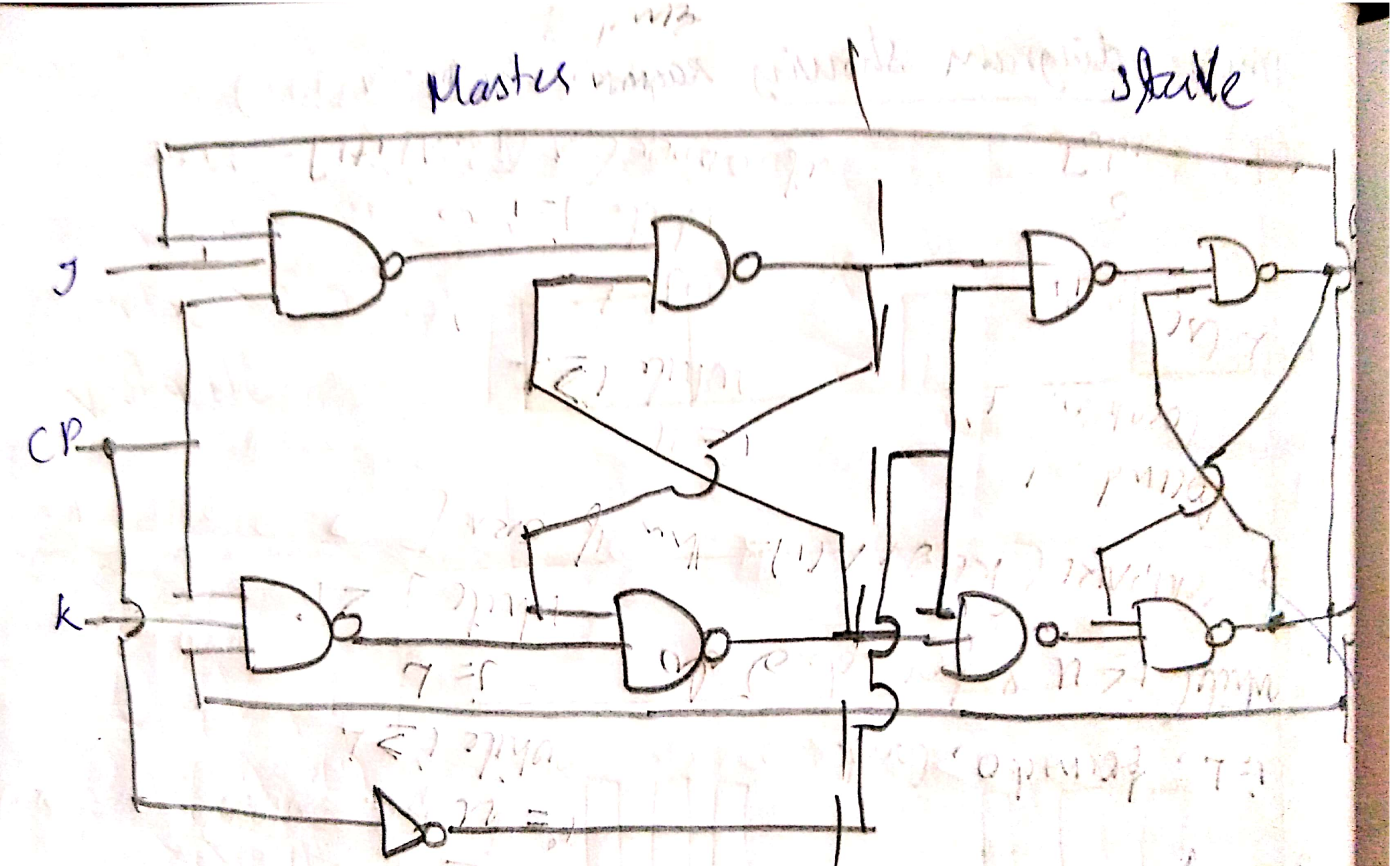
JK, K=1, CP=1

Timing diagram showing race



Methods to avoid racing Racing.

1) Half time period should be less than propagation delay. And thus CP can be made 0;
∴ Use +ve or -ve edge triggered flipflop
2. Master-slave flipflop

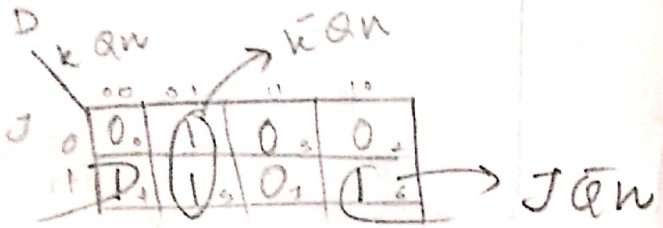


1. Implement JK flipflop using D flipflop

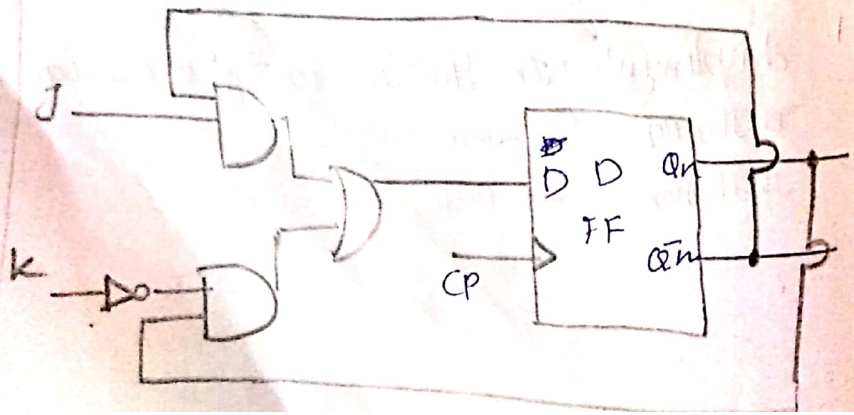
D-flipflop - excitation table

JK flipflop - truth table

JK Input		Output		D input
J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

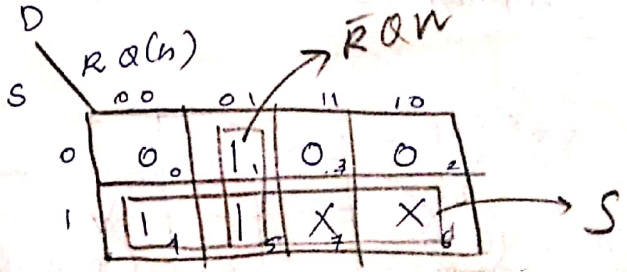


$D = \bar{K} Q_n + J \bar{Q}_n$

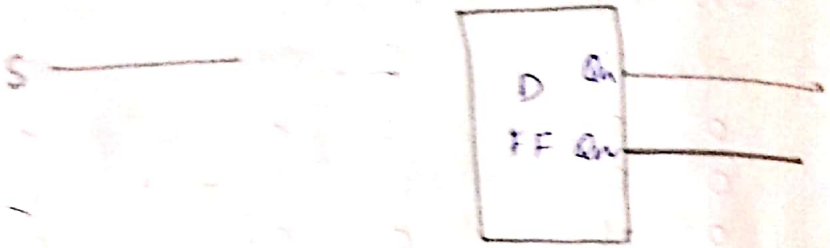


2. Implement SR flipflop using D flip flop.

SR Input		Output		D input
S	R	Qn	Qn+1	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	0	0	X	X
1	1	1	X	X



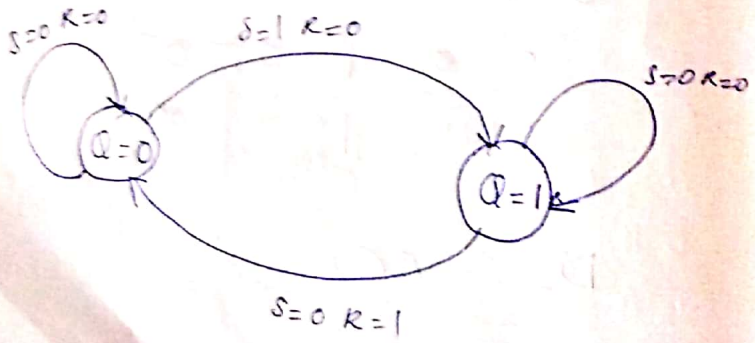
$D = S + \bar{R} Q_n$



2. Convert JK flipflop to T flipflop

State Table, state diagram, State equation

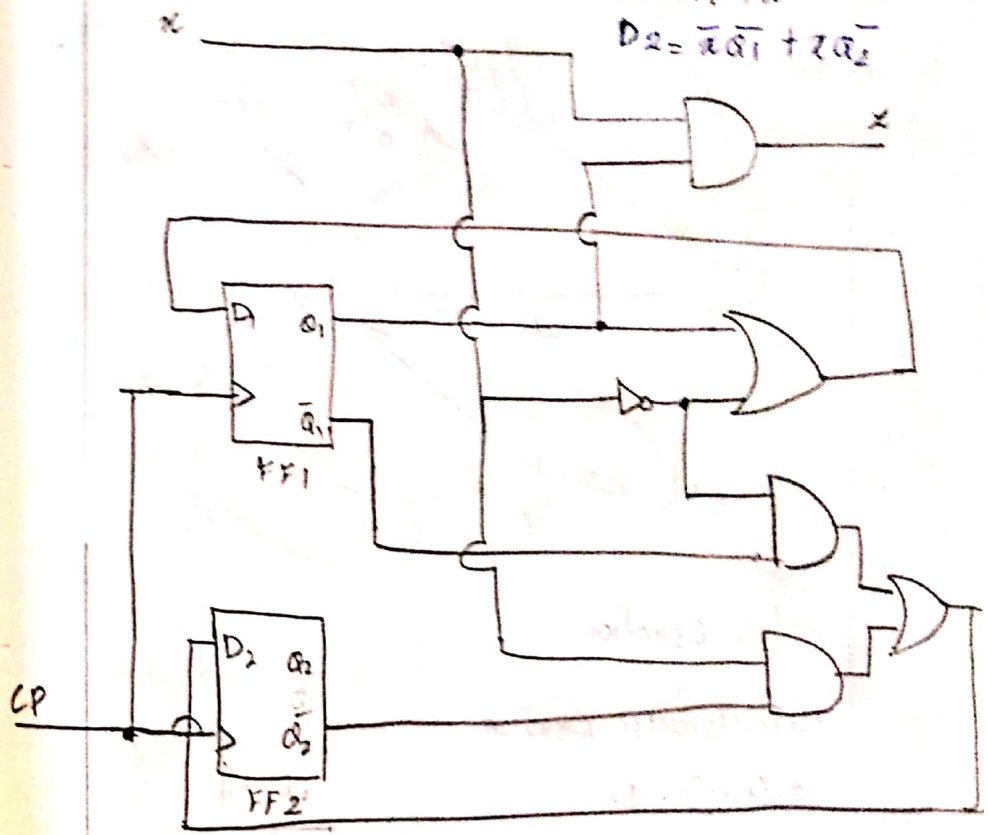
S-R flipflop



$Z = x Q_1$

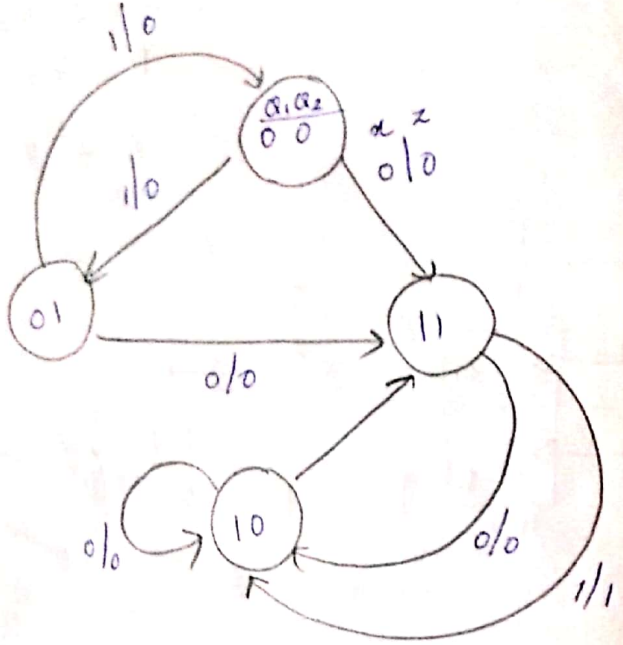
$D_1 = Q_1 + x$

$D_2 = \bar{x} Q_1 + x \bar{Q}_2$



Present state Q_1	Present state Q_2	Next state $x=0$	Next state $x=1$	Output Z $x=0$	Output Z $x=1$
0	0	1 1	0 1	0	0
0	1	1 1	0 0	0	0
1	0	1 0	1 1	0	1
1	1	1 0	1 0	0	1

State Diagram



State Equation:

Characteristic Equation:

$Q_1(t+1) = D_1$

$Q_2(t+1) = D_2$

State Equation:

$Q_1(t+1) = Q_1(t) + \bar{x}$

$Q_2(t+1) = \bar{x}\,\overline{Q_1(t)} + x\,\overline{Q_2(t)}$

⇒ Design a sequential circuit with 4 flipflop A, B, C, D. Next states of B, C, D are equal to the present states of A, B and C respectively. The next state of A is equal to the XOR of the present states of C and D. Implement the circuit with D flipflop.

$Q_A(t+1) = Q_C(t) + Q_D(t)$

$Q_B(t+1) = Q_A(t)$

$Q_C(t+1) = Q_B(t)$

$Q_D(t+1) = Q_C(t)$

$Q(t+1) = D$

$D_A = Q_C(t) \oplus Q_D(t)$

$D_B = Q_A(t)$

$D_C = Q_B(t)$

$D_D = Q_C(t)$

V_IMP

=> Design a sequential circuit with JK flip flop to satisfy the following equations

$A(t+1) = \bar{A}B\bar{C}D + \bar{A}B\bar{C} + AC\bar{D} + A\bar{C}\bar{D}$

$B(t+1) = \bar{A}C + C\bar{D} + \bar{A}B\bar{C}$

$C(t+1) = B$

$D(t+1) = \bar{D}$

Characteristic equation

$Q(t+1) = J\bar{Q}(t) + \bar{K}Q(t)$

$A(t+1) = JA\bar{A} + k\bar{A}A$

$A(t+1) = (\bar{B}CD + \bar{B}\bar{C})\bar{A} + (CD + \bar{C}\bar{D})A$

$JA \qquad\qquad k\bar{A}$

$JA = (\bar{B}CD + \bar{B}\bar{C}) = \bar{B}C[D+1] = \underline{\bar{B}C}$

$kA = \overline{(CD + \bar{C}\bar{D})}$

$B(t+1) = JB\bar{B} + k\bar{B}B$

$B(t+1) = \bar{A}C(B+\bar{B}) + C\bar{D}(B+\bar{B}) + \bar{A}B\bar{C}$

$= \bar{A}CB + \bar{A}C\bar{B} + C\bar{D}B + C\bar{D}\bar{B} + \bar{A}B\bar{C}$

$= B(\bar{A}C + C\bar{D}) + \bar{B}(\bar{A}C + C\bar{D}) + \bar{A}\bar{C}$

~~$JB = C$~~

$= B(\bar{A}C + C\bar{D} + \bar{A}\bar{C}) + \bar{B}(\bar{A}C + C\bar{D})$

JB
$\bar{A}B + B\bar{C}$

$JB = \bar{A}C + C\bar{D}$

$KB = \overline{\bar{A} + C\bar{D}} = \bar{\bar{A}} \cdot \overline{C\bar{D}}$

$= A \cdot (C + D)$ //

$C(t+1) = JC\,\bar{C} + \bar{K}C\,C$

$C(t+1) = BC + B\bar{C}$

$JC\,\bar{C} = B\bar{C}$

$\bar{K}C\,\bar{C} = BC$

$JC = B$

$\bar{K}C = B$

$JC = B$

$K\bar{C} = \bar{B}$

$D(t+1) = \bar{D}$

$D(t+1) = JD\bar{D} + \bar{K}\bar{D}D$

$\bar{D} \cdot 1 + 0 \cdot D$

$JD = 1 \quad \bar{K}D = 0$

$JD = 1 \quad KD = 1$ //

State Reduction and Assignment

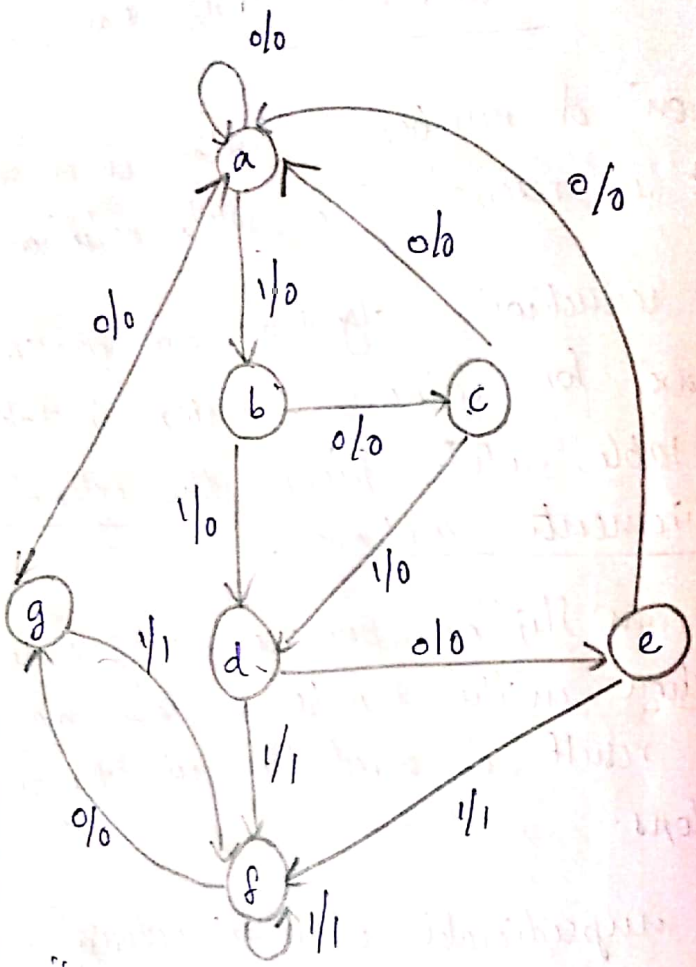
Reduction of number of flipflops in a sequential circuit is referred to as state reduction problems.

State reduction algorithms are concerned with procedure for reducing number of states in a state table, while keeping the external i/p, o/p requirements unchanged.

Since m flipflops produce 2^m states, a reduction in the number of states may or may not result in a reduction in the no: of the flipflops.

An unpredictable effect in reducing number of flipflops is that sometimes equivalent circuit with less flipflops may require more combinational gates.

flipflops states
$m \rightarrow 2^m$



i/p o/p relation

input	-	0	1	0	1	0	1	1	0	1	0	0
state	-	a	a	b	c	d	e	f	f	g	f	g
o/p	-	0	0	0	0	0	1	1	0	1	0	0

Two states are said to be equivalent for each member of set of i/p s they give exactly the same o/p and send the circuit either to the same state or to an equivalent state. When 2 states are equivalent one of them can be removed without altering the i/p o/p relationship.

State Table

present state	next state x=0	next state x=1	output x=0	output x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
*d	e	f	0	1
e	a	f	0	1
*f	g e	f	0	1
g	a	f	0	1

e and g are equivalent state. ∴ we can remove one state i, suppose we remove 'g'.

d and f are equivalent

∴ Remove f

Reduced state Table

present state	next state x=0	next state x=1	o/p x=0	o/p x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

i/p o/p relation

i/p - 0 1 0 1 0 1 1 0 1 0 0

state - a b c d e

o/p -